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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,205	11/26/2003	Lawrence Pileggi	361007.000035	1204

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,205	PILEGGI ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed November 26, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Kirihata et al. US Pat no. 5,764,655.

As per claim 1:

Kirihata et al. teaches a system to test integrated circuits on a wafer (Figure 4 # 21), comprising: a transceiver formed on the wafer (Figure 4 #26, column 5, lines 49-56); and an antenna system couplable to the transceiver (column 6, lines 59-61).

As per claim 2:

Kirihata et al. teaches the system, wherein the transceiver is couplable to a plurality of integrated circuits formed on the wafer (Figure 4 # 22, 23, & 24) to test selected ones of the plurality of integrated circuits (Figure 4 # 22, column 6, lines 61-67).

As per claim 3:

Kirihata et al. teaches the system of claim 2, wherein the transceiver is adapted to apply test signals to at least one selected integrated circuit (Figure 4 # 22, column 6, lines 66-67) of the plurality of integrated circuits to test the at least one selected integrated circuit in response to the antenna system receiving a signal (column 6, lines 59-65).

As per claim 4:

Kirihata et al. teaches the system of claim 2, wherein the antenna system is adapted to transmit signals corresponding to results from testing at least one selected integrated circuit of the plurality of integrated circuits (column 7, lines 1-5).

As per claim 5:

Kirihata et al. teaches the system of claim 2, further comprising a multiplexing circuit (Figure 2 "MUX", column 2, lines 30-35) to couple the transceiver to each of the plurality of integrated circuits.

As per claim 6:

Kirihata et al. teaches the system of claim 1, wherein the antenna system comprises one of a loop antenna (column 6, lines 59-61), a pair of dipole

antennas or an antenna array formed by loop (column 6, lines 59-61) or dipole antenna elements.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-19 & 30-34 are rejected under 35 U.S.C. 102(a) as being fully anticipated by Tuttle et al. US Patent no. 5,983,363 B1.

As per claim 1:

Tuttle et al. teaches a system to test integrated circuits on a wafer (Figure 1 # 10), comprising: a transceiver formed on the wafer (Figure 3 # 12, column 5, lines 53-54); and an antenna system couplable to the transceiver (column 5, lines 54-56).

As per claim 7 & 30:

Tuttle et al. teaches the system of claim 1, further comprising: a plurality of transceivers (column 1, lines 63-67), each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer (column 2, lines 36-39) and each of the transceivers being formed at a different location on the wafer (Figure 1 # 12); and a plurality of antenna systems, each antenna system being coupleable to at least one of the plurality of

transceivers (column 2, lines 2-4) and each of the plurality of antenna systems being formed at different locations on the wafer (Figure 1 # 12).

As per claim 8 & 32:

Tuttle et al. teaches the system of claim 7, wherein each transceiver of the plurality of transceivers or each transceiver in a subset of transceivers of the plurality of transceivers are each adapted to transmit test result signals simultaneously on different radio frequencies (column 2, lines 36-39).

As per claim 9:

Tuttle at al. teaches the system of claim 7, wherein each of the antenna systems is formed to minimize electromagnetic interference with the multiplicity of integrated circuits during testing (column 2, lines 10-16).

As per claim 10 & 33:

Tuttle et al. teaches the system of claim 7, wherein each of the transceivers and antenna systems are formed in a predetermined distribution on the wafer (Figure 4)

As per claim 11:

Tuttle et al. teaches the system of claim 10, wherein the predetermined distribution is adapted to minimize space utilization, facilitate optimum testing of a selected number of integrated circuits simultaneously (column 5-6, lines 60-59), and to minimize electromagnetic interference with the integrated circuits during testing and between different transceivers and associated antenna systems (column 2, lines 10-16).

As per claim 12 & 31:

Tuttle et al. teaches the system of claim 7, further comprising a multiplexing circuit (Figure 3 # 122), wherein an integrated circuit to be test and an associated transceiver are selectable by at least one of a word-line or a bit-line and wherein the transceiver is adapted to select a proper stream of test data of the integrated circuit under test from the multiplexing circuit (column 5, lines 15-37).

As per claim 13 & 34:

Tuttle et al. teaches the system of claim 7, further comprising a word-line/bit-line power distribution scheme adapted to select an integrated circuit to be tested and an associated transceiver and to distribute test mode power to the selected integrated circuit to be tested and the associated transceiver (column 5, lines 39-48).

As per claim 19:

Tuttle et al. teaches the system of claim 1, wherein the transceiver is adapted to receive and to transmit signals to perform real-time tests periodically during fabrication of the wafer (column 5, lines 23-37).

As per claim 30:

Tuttle et al. teaches a system to test integrated circuits on a wafer, comprising: a plurality of transceivers (column 1, lines 63-67) each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer (column 2, lines 36-39) and each of the transceivers being formed at a different location on the wafer in one of a plurality of scribe lines formed in the wafer or at other locations on the wafer (Figure 1 # 12); and at

least one antenna systems couplable to the plurality of transceivers (column 2, lines 2-4).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 14-20, 31, 35, & 42 are rejected under 35 U.S.C. 102(a) as being fully anticipated by Schmidt US PG-Pub No. 20020196029 A1.

As per claim 1:

Schmidt teaches a system to test integrated circuits on a wafer (Figure 1 # 10), comprising: a transceiver formed on the wafer (Figure 1 # 18); and an antenna system couplable to the transceiver (Figure 4 # 193, paragraph [0046]).

As per claim 7 & 31:

Schmidt teaches the system of claim 1, further comprising: a plurality of transceivers, each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer and each of the transceivers being formed at a different location on the wafer and a plurality of antenna systems, each antenna system being coupleable to at least one of the

plurality of transceivers and each of the plurality of antenna systems being formed at different locations on the wafer (Figure 1).

As per claim 14 & 35:

Schmidt teaches the system of claim 1, wherein the transceiver receives power via one of a probe (Figure 3 # 208, paragraph [0021]), a radio frequency power signal (paragraph [0046]), a word-line or a bit-line, and a pad electrically connectable to the transceiver, wherein the pad is connectable to an external power source (Figure 4 # 195, paragraph [0046]).

As per claim 15:

Schmidt teaches the system of claim 1, further comprising a pad formed proximate to a periphery of the wafer and electrically connectable to the transceiver to provide power to the transceiver (paragraph [0045]).

As per claim 16:

Schmidt teaches the system of claim 1, further comprising another transceiver (Figure 1 # 24) and test unit (Figure 1 # 22) external to the wafer and adapted to transmit scan test vectors to the transceiver on the wafer and to receive test results from the transceiver on the wafer (paragraph [0018]).

As per claim 17:

Schmidt teaches the system of claim 16, wherein the transceiver is adapted to transmit self-test data and to receive and transmit scan test vectors from the external transceiver and test unit (Figure 1 # 22, paragraph [0018]).

As per claim 18:

Schmidt teaches the system of claim 1, wherein the transceiver is adapted to provide one of an amplitude shift keying (ASK) or an on-off keying (OOK) modulation scheme (Figure 4 # 116, paragraph [0043]).

As per claim 20:

Schmidt teaches the system of claim 1, wherein the transceiver is adapted to receive and to transmit signals to perform real-time tests periodically during fabrication of the wafer (paragraph [0008]).

As per claim 28:

Schmidt teaches the system of claim 1, wherein the antenna system comprises an antenna external to the wafer and wherein the transceiver is connectable to the antenna by a wafer boat or fixture (Figure 1 # 20 paragraph [0019]).

As per claim 29 & 42:

Schmidt teaches The system of claim 1, further comprising: an insulative layer formed on the wafer; and a conductive layer formed on the insulative layer and electrically connecting to the transceiver via an opening formed in the insulative layer to test selected ones of the integrated circuits during manufacturing, wherein the insulative layer and the conductive layer are removable for further fabrication of the integrated circuits (paragraph [0021], this is the basic structure of any wafer).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21, 36, 43 & 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt US PG-Pub No. 20020196029 A1 and further in view of Kirihata et al. US Pat no. 5,764,655.

As per claim 21, 36:

Schmidt substantially teaches the system as rejected in claim 1, wherein the transceiver comprises: a down converter to convert a received radio frequency (RF) signal to an intermediate frequency (IF) signal (paragraph [0042], lines 7-10); a received signal strength indicator (RSSI) (paragraph [0042], lines 7-10); a limiting amplifier to amplify the IF signal in response to the RSSI (paragraph [0042], lines 11-15).

Schmidt does not explicitly teach a comparator to generate a data signal in response to the amplified IF signal.

However Kirihata et al. in an analogous art teaches a comparator embedded in the RF Wand or the chip (column 7, lines 1-5). It would have been obvious to one of ordinary skill in the art to incorporate a comparator within the teachings of Schmidt, since one of ordinary skill in the art would have realized that incorporating a comparator would have allowed for only the transmission of the test results, which are different from the ones stored in the memory. Further it should be noted that the function of generating a data signal in response to the amplified IF signal is already being performed in Schmidt (paragraph [0042], lines 11-15), it is only that Schmidt does not explicitly state the apparatus that is performing the above function.

As per claim 43 & 44:

Schmidt substantially teaches the system a transceiver comprising: a down converter to convert a received radio frequency (RF) signal to an intermediate frequency (IF) signal (paragraph [0042], lines 7-10); a received signal strength indicator (RSSI) (paragraph [0042], lines 7-10); a limiting amplifier

to amplify the IF signal in response to the RSSI (paragraph [0042], lines 11-15), wherein each of the down converter, RSSI, amplifier and comparator are formed in a scribe line formed in the wafer (Figure 1).

Schmidt does not explicitly teach a comparator to generate a data signal in response to the amplified IF signal.

However Kirihata et al. in an analogous art teaches a comparator embedded in the RF Wand or the chip (column 7, lines 1-5). It would have been obvious to one of ordinary skill in the art to incorporate a comparator within the teachings of Schmidt, since one of ordinary skill in the art would have realized that incorporating a comparator would have allowed for only the transmission of the test results, which are different from the ones stored in the memory. Further it should be noted that the function of generating a data signal in response to the amplified IF signal is already being performed in Schmidt (paragraph [0042], lines 11-15), it is only that Schmidt does not explicitly state the apparatus that is performing the above function.

Claims 22 & 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt US PG-Pub No. 20020196029 A1 and further in view of Menich et al. US Pat no. 4,704,734.

As per claim 22 & 37:

Schmidt substantially teaches the system as rejected in claim 1 above, wherein the transceiver comprises a filter to filter selected frequency band signals (paragraph [0040], lines 1-12); a voltage controlled oscillator to receive a filtered signal from the filter (paragraph [0042], lines 1-6); and a power amplifier

to modulate a carrier signal from the voltage controlled oscillator by a data input signal (paragraph [0042], lines 11-15).

Schmidt does not explicitly teach a phase/frequency detector to receive an input or reference signal and a charge pump to receive.

However, Menich et al. in an analogous art teaches a phase/frequency detector to receive an input or reference signal and a charge pump to receive (column 7, lines 1-65). Therefore it would have been obvious to one of ordinary skill in the art to use the operating procedure of the transceiver as described by Menich et al. in Schmidt's invention, since doing so would have enables Schmidt's invention to test multiple circuits at different frequencies with minimum interference. Further it should be noted that Schmidt does not go in detail in explaining the method of operation of the transceiver but the procedure disclosed in paragraphs [0040-0042] is essentially the same as disclosed in the above claim. Hence, it would be obvious to interpret the procedure of the above claim from Schmidt itself, without using Menich et al.

Claims 45 & 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schmidt US PG-Pub No. 20020196029 A1, in view of Kirihata et al. US Pat no. 5,764,655 and further in view of Menich et al. US Pat no. 4,704,734.

As per claims 45 & 46:

Schmidt substantially teaches the system as rejected in claim 43 above, wherein the transceiver comprises a filter to filter selected frequency band signals (paragraph [0040], lines 1-12); a voltage controlled oscillator to receive a

filtered signal from the filter (paragraph [0042], lines 1-6); and a power amplifier to modulate a carrier signal from the voltage controlled oscillator by a data input signal (paragraph [0042], lines 11-15), wherein each of the phase/frequency detector, charge pump, filter, voltage controlled oscillator and power amplifier are formed in a scribe line formed in the wafer (Figure 1).

Schmidt does not explicitly teach a phase/frequency detector to receive an input or reference signal, a charge pump to receive and a comparator to generate a data signal in response to the amplified IF signal.

Menich et al. in an analogous art teaches a phase/frequency detector to receive an input or reference signal and a charge pump to receive (column 7, lines 1-65). Therefore it would have been obvious to one of ordinary skill in the art to use the operating procedure of the transceiver as described by Menich et al. in Schmidt's invention, since doing so would have enables Schmidt's invention to test multiple circuits at different frequencies with minimum interference. Further it should be noted that Schmidt does not go in detail in explaining the method of operation of the transceiver but the procedure disclosed in paragraphs [0040-0042] is essentially the same as disclosed in the above claim. Hence, it would be obvious to interpret the procedure of the above claim from Schmidt itself, without using Menich et al.

Kirihata et al. in an analogous art teaches a comparator embedded in the RF Wand or the chip (column 7, lines 1-5). It would have been obvious to one of ordinary skill in the art to incorporate a comparator within the teachings of Schmidt, since one of ordinary skill in the art would have realized that

incorporating a comparator would have allowed for only the transmission of the test results, which are different from the ones stored in the memory. Further it should be noted that the function of generating a data signal in response to the amplified IF signal is already being performed in Schmidt (paragraph [0042], lines 11-15), it is only that Schmidt does not explicitly state the apparatus that is performing the above function.

Claims 23, 24, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. US Patent no. 5,983,363 B1.

As per claims 23, 24 & 39:

Tuttle et al. substantially teaches the system as rejected in claim 1 above.

Tuttle et al. does not explicitly teach the system, wherein the transceiver and the wafer are formed in one of a scribe line on the wafer.

However, Tuttle et al. teaches the system, wherein the transceiver and antenna are formed in a cavity isolated from the rest of the circuitry (Figure 4 # 71, column 5, lines 55-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use form the transceiver and the antenna on the scribe line instead of the cavity, since the examiner takes Official Notice of the equivalence of scribe and cavity for their use in the art and within the level of ordinary skill in the art.

Claims 25, 40, 41, 47, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. US Patent no. 5,983,363 B1, in view of Schmidt US PG-Pub No. 20020196029 A1 and further in view of Kirihata et al. US Pat no. 5,764,655.

Tuttle et al. teaches the system of claim 24 as shown in the rejection above.

Tuttle et al. does not explicitly teach the exact use of amplifiers or loop antennas.

Schmidt in an analogous art teaches a plurality of differential amplifier circuits, each differential amplifier circuit being associated with one of the plurality of transceivers, wherein only one of the plurality of differential amplifier circuits is active at any given time to permit the associated transceiver to receive or transmit signals (paragraph [0042]). It would have been obvious to one of ordinary skill in the art to use amplifiers within the teaching of Tuttle et al. since one of ordinary skill in the art would have recognized that using an amplifier would have strengthened the testing signal in Tuttle et al.'s invention.

Kirihata et al. in an analogous art teaches a loop antenna adapted to be shared by a plurality of transceivers (column 6, lines 59-61). It would have been obvious to one of ordinary skill in the art to use the loop antennas within the teaching of Tuttle et al. since one of ordinary skill in the art would have recognized that using a loop antenna would have enabled the testing device to phase out unwanted noise or an unwanted other signal coming from a different direction because a loop antenna is insensitive to localized electric field noise. Further it should be noted that Tuttle et al. and Schmidt are already using an antenna in their invention, but they have not specified which exact kind. Since a loop antenna falls under the general category of antenna, it should be noted that the above rejection is further strengthened due to this observation.

Claims 26, 27, 49, 50 & 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. US Patent no. 5,983,363 B1 and further in view of Terranova et al US PG-Pub no. 20020160722 A1.

As per claim 26 & 49:

Tuttle et al. teaches the system of claim 24 as shown in the rejection above.

Tuttle et al. does not explicitly teach an antenna system wherein the antenna further comprises an inductor connected in parallel with each differential amplifier.

However, Terranova et al. in an analogous art teaches the antenna system further comprises an inductor connected in parallel (paragraph [0084]) with each differential amplifier circuit (paragraph [0089]), wherein the inductor completes the loop antenna when an associated differential amplifier circuit is disabled (paragraph [0090-0105]). It would have been obvious to one of ordinary skill in the art to use a an inductor and amplifier circuit within the teachings of Tuttle et al., since one of ordinary skill in the art would have recognized that functioning of loop antenna depends on inductance and hence even though Tuttle et al. does not explicitly explain the structure of the antenna in his invention, a loop antenna would fall under the category of an antenna.

As per claim 27, 50 & 51:

Tuttle et al. teaches the system of claim 24 as shown in the rejection above.

Tuttle et al. does not explicitly teach an antenna system wherein the antenna further comprises an inductor connected in parallel with each differential amplifier and including a FET to couple a voltage source.

However, Terranova et al. in an analogous art teaches the antenna system further comprises an inductor connected in parallel (paragraph [0084]) with each differential amplifier circuit (paragraph [0089]), wherein the inductor completes the loop antenna when an associated differential amplifier circuit is disabled (paragraph [0090-0105]) and a field effect transistor (FET) to couple a voltage source to a node between each pair of inductors, wherein the voltage source is connected to the node in response to an RF carrier signal from an associated one of the plurality of transceivers being applied to a gate of the FET (paragraph [0090]), wherein the loop antenna is physically small compared to a wavelength at which the loop antenna operates (paragraph [0160-0181]). It would have been obvious to one of ordinary skill in the art to use a an inductor, amplifier circuit and a FET within the teachings of Tuttle et al., since one of ordinary skill in the art would have recognized that functioning of loop antenna depends on inductance and the use of a FET allows for fast switching times, hence even though Tuttle et al. does not explicitly explain the structure of the antenna in his invention, a loop antenna would fall under the category of an antenna.

As per claim 52-70:

These claims are directed to a method of the system of Claims 1-51. Schmidt, Kirihata et al., Menich et al., Tuttle et al., Terranova et al., either alone

or in combination as stated above, teach the system as set forth in Claims 1-51. Therefore, Schmidt, Kirihata et al., Menich et al., Tuttle et al., Terranova et al., also teach, either alone or in combination as stated above, the method as set forth in claims 52-70.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (6794310 B1 6487681 B1, 3091734 A, 5448110 A, 6268774 B1, 5003316 A, 5437057 A, 4609911 A) mention the same wafer testing procedure which includes the use of transceivers and antennas included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS
Saqib Siddiqui
Art Unit 2138
02/21/2006

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